

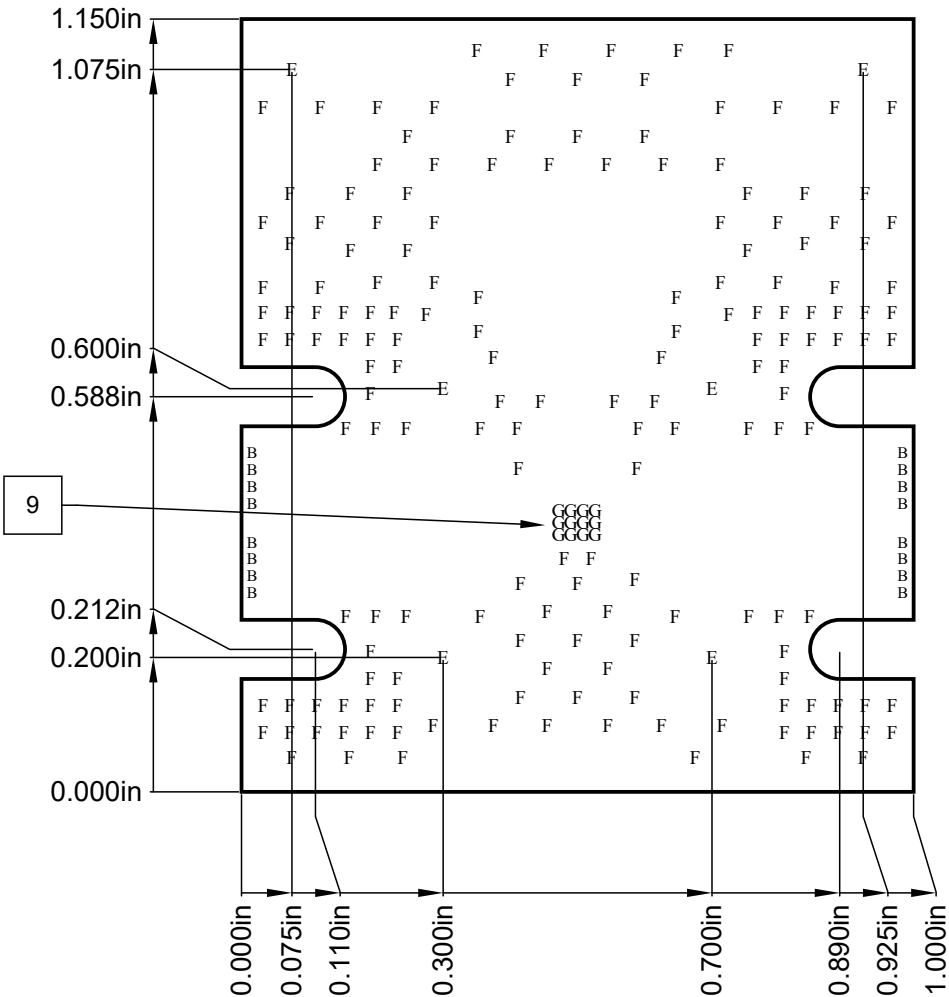
NOTES (UNLESS OTHERWISE SPECIFIED):


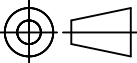
1. BOARD FABRICATION METHODS MUST COMPLY WITH:
FABRICATE IN ACCORDANCE WITH IPC-6018B, per IPC-6011, CLASS 2.
2. ARTWORK FORMAT: GERBER 274X
GERBER DATA SUPPLIED WITH DESIRED FINAL TRACE WIDTHS. PROCESS
COMPENSATION TRACE WIDTH ADJUSTMENTS TO BE DONE BY PCB FABRICATOR
3. MATERIAL:
NUMBER OF LAYERS: 2 LAYERS
METAL 1 0.5oz. (PLATE TO 1.0oz)
CORE 1: ROGERS 4003C, .008in. THICK
METAL 2 0.5oz. (PLATE TO 1.0oz)
SOLDERMASK TOP: LPI (LIQUID PHOTO-IMAGEABLE), GREEN OR LDI (LASER DIRECT IMAGEABLE), GREEN. MAX FINISH
THICKNESS OF SOLDERMASK TO BE 0.001in.
SILKSCREEN TOP: HIGH TEMPERATURE, NON-CONDUCTIVE, WHITE EPOXY BASED INK.
4. FINISH PLATING:
A. METAL 1(TOP) AND METAL 2(BOTTOM):
ELECTROLYTIC FLASH GOLD
NICKEL PLATE per QQ-N-290, CLASS 1, GRADE G, 200µin. (5µm)
GOLD PLATE per ASTM B 488, TYPE III, CODE A, 3-10µin. (0.08-0.25µm)

B. METAL 1(TOP) SELECTIVE ELECTROLYTIC FLASH GOLD PLATING:
GOLD PLATE per ASTM B 488, TYPE III, CODE A, CLASS 1, 50µin. (1.27µm)
PLATING MUST BE FREE FROM CONTAMINATION, STAINS AND DEBRIS.
5. FINISHED BOARD THICKNESS: (0.011in) ±.003IN.
6. COPPER IS PULLED BACK 0.002in. FROM EDGE OF BOARD ON METAL 1 (TOP) AND METAL 2 (BOTTOM).
7. TOLERANCE: PC BOARD OUTLINE: ±0.002in.
8. BURRS SHALL NOT EXCEED 0.002in.
- 9 VIA PLATING/FILLING:
A. ALL 8 MIL (A) VIAS UNDER THE DUT ARE TO BE COPPER-FILLED, OVER-PLATED AND PLANARIZED.
FINISHED COPPER THICKNESS TO BE 0.0014 ±0.0004in.
B. ALL OTHER PLATED THRU HOLES TO BE PLATED TO 0.0007in. MIN. THICKNESS.
10. METAL 1(TOP) AND METAL2(BOTTOM) AFTER OVERPLATING AND PLANARIZATION SHALL HAVE A MAX
ALLOWABLE NEGATIVE FEATURE OF 0.0008in. AND A MAX ALLOWABLE POSITIVE FEATURE OF 0.0003in.
11. CONDUCTOR WIDTHS AND SPACING TO BE WITHIN 0.003in. OF CAD DATABASE.
12. SOLDERMASK IN PLATED-THRU HOLES IS ACCEPTABLE AS LONG AS IT DOES NOT EXIST ON BACKSIDE OF BOARD.
13. ALL HOLES TO BE LOCATED WITHIN ±0.003 OF CAD DATABASE.
14. NO VENDOR MARKING OR SERIALIZATION ALLOWED.
15. DELIVER BOARDS BAGGED AS SINGLES
16. NO ELECTRICAL TEST NEEDED.

REVISION HISTORY			
REV	DESCRIPTION	DATE	APPROVAL
A	NEW RELEASE	8/31/18	O.MARRUFO

DUT AREA/COPPER-FILLED



UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES		SAP NO. 285006				
TOLERANCES .XX = ±.01 .XXX = ±.005 .XXXX = ±.0010 ANGLES = ± 0.5°		APPROVAL AND RELEASE RECORDS MAINTAINED IN PDE				DATE
 THIRD ANGLE PROJECTION DO NOT SCALE DRAWING		DESIGNER	O.MARRUFO	7/11/18		
		ENGR.	M.ROBERG	7/11/18		
		MFG	PDE CONTROLLED			
		MANAGER				
		Q.A.				
		CAGE CODE	1CVM1			
		SIZE		DWG. NO.		REV.
		B		QPA2225D-4000		A
		SCALE: 1:1		SHEET 1 OF 4		

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Layer Stack Legend

	Material	Layer	Thickness	Dielectric	Material Type
		SILKSCREEN_TOP			Legend
	Surface Material	SOLDERMASK_TOP	0.4mil	Solder Resist	Solder Mask
	Copper	METAL1_TOP	0.7mil		Signal
	Core		8.0mil	ROGERS 4003C	Dielectric
	Copper	METAL2_BOT	0.7mil		Signal
Total thickness: 9.8mil					

Drill Table

Symbol	Count	Hole Size	Plated	Via / Pad	Drill Layer Pair
G	12	8.00mil(0.20mm)	Plated	Via	METAL1_TOP - METAL2_BOT
B	16	15.00mil(0.38mm)	Plated	Via	METAL1_TOP - METAL2_BOT
F	171	20.00mil(0.51mm)	Plated	Via	METAL1_TOP - METAL2_BOT
E	6	100.00mil(2.54mm)	Plated	Pad	METAL1_TOP - METAL2_BOT

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SIZE	CAGE CODE	DWG. NO.	REV.
B	1CVM1	QPA2225D-4000	A
SCALE: 1:1		SHEET 2 OF 4	

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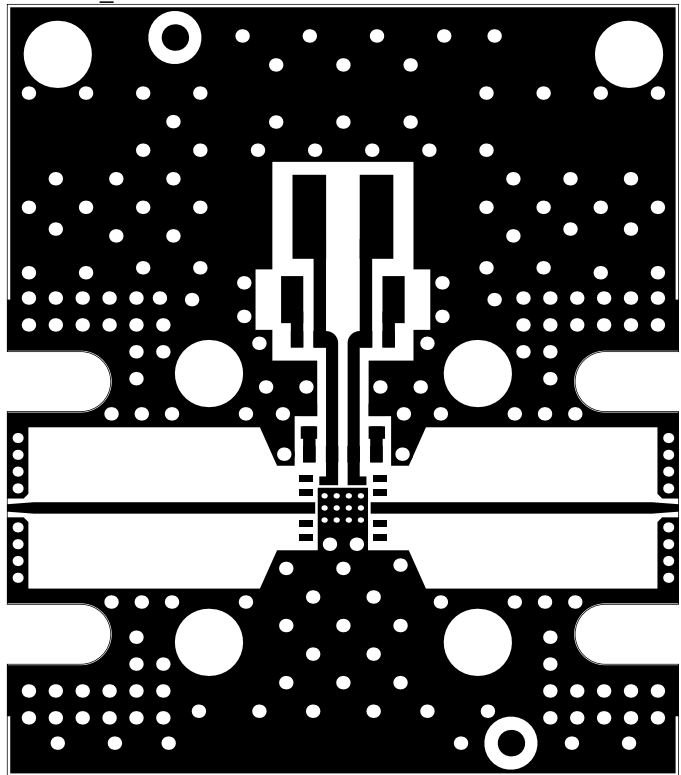
B

B

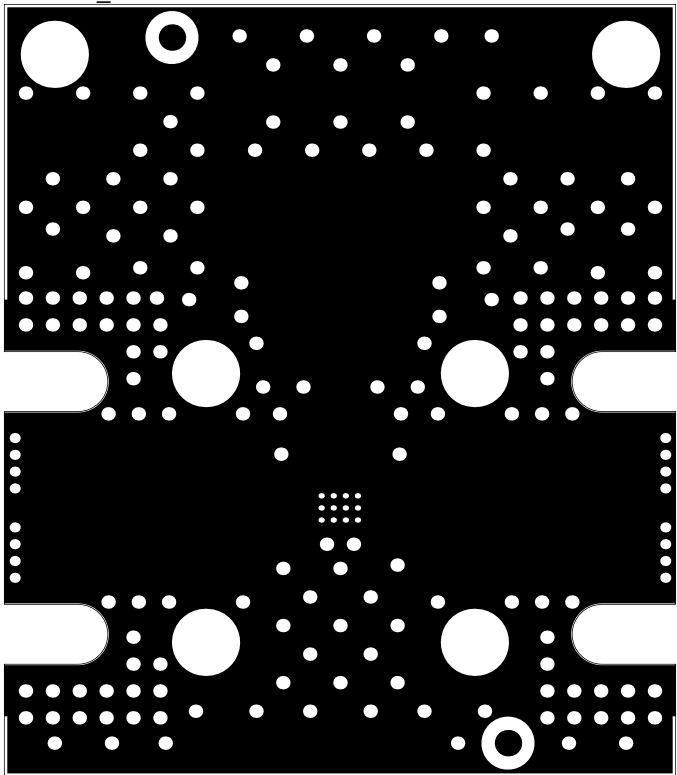
A

A

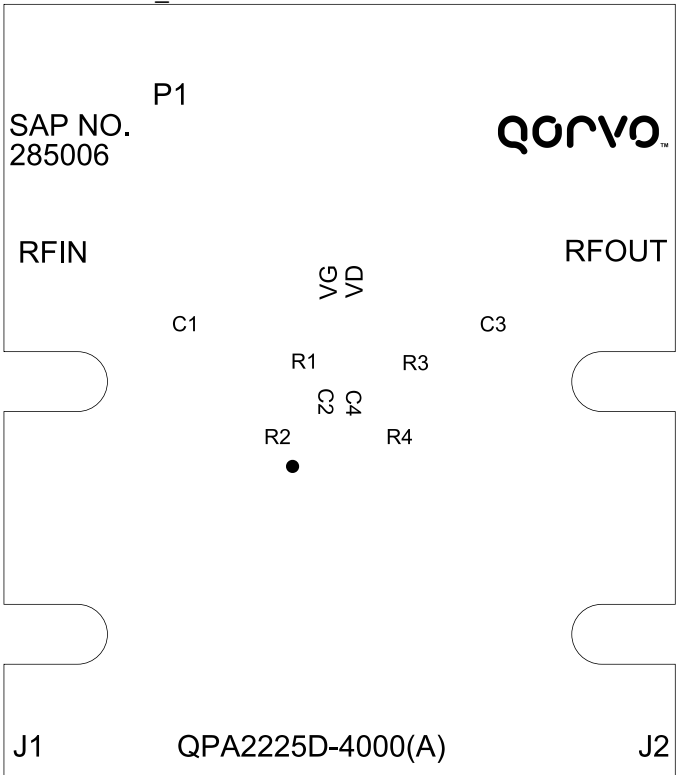
METAL1_TOP



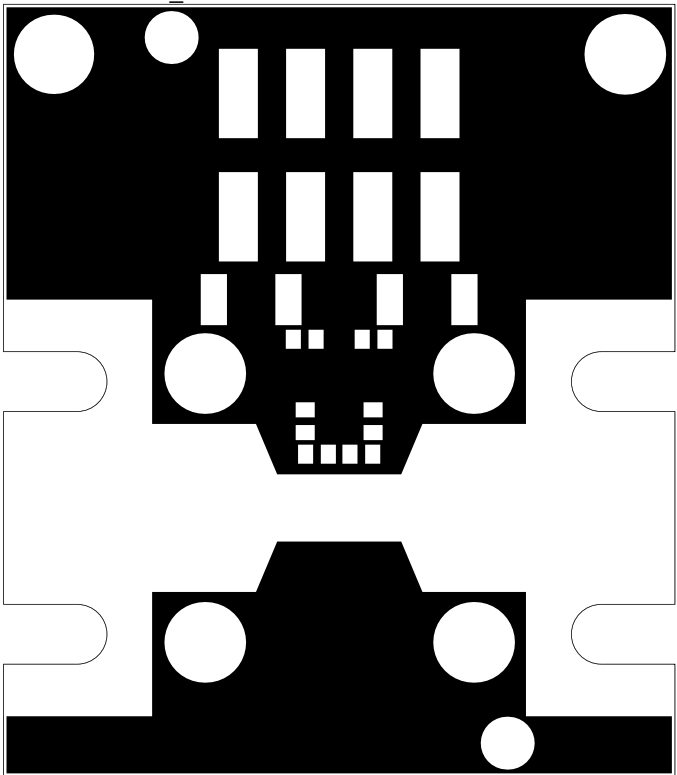
METAL2_BOT



SILKSCREEN_TOP



SOLDERMASK_TOP



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SIZE	CAGE CODE	DWG. NO.	REV.
B	1CVM1	QPA2225D-4000	A
SCALE:	1:1	SHEET 3 OF 4	

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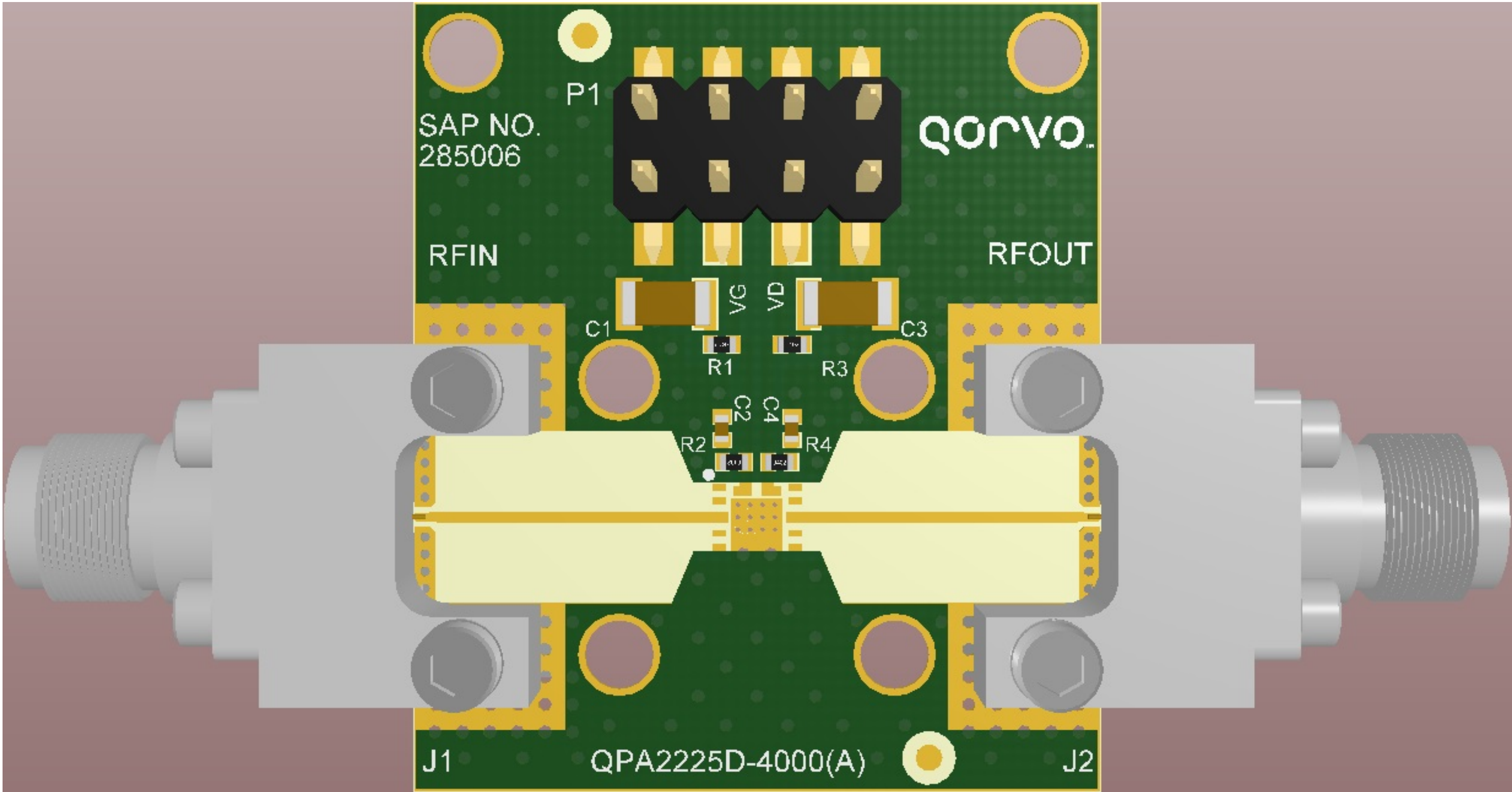
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SIZE	CAGE CODE	DWG. NO.	REV.
B	1CVM1	QPA2225D-4000	A
SCALE:	1:1	SHEET 4 OF 4	

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